PENDING CLAIMS AND STATUS THEREOF

Claims 1-6 (canceled)

7. (original allowed): Counter arrangement comprising:

- a control unit;

- first, second, and third registers coupled with said control unit;

- fourth, fifth, and sixth registers coupled with said control unit;

- first, second, and third functional units each having two inputs and an output; wherein

- the inputs of the first functional unit being coupled with the first and second register, respectively and the output with the fourth register;

- the inputs of the second functional unit being coupled with the second and third register, respectively and the output with the fifth register;

- the inputs of the third functional unit being coupled with the first and third register, respectively and the output with the sixth register; and wherein

the control unit performs a counter function on the first, second, and third registers such that the content of only one of the counter registers changes for each change in a counting sequence.

8. **(currently amended)** Counter arrangement according to claim **[[1]]** 7, wherein the functional units perform a logical function.

9. **(currently amended)** Counter arrangement according to claim **[[1]]** 7, wherein the functional units perform an arithmetic function.

10. (original allowed): Counter arrangement according to claim 7, wherein the functional units are EXCLUSIVE OR gates.

11. (original allowed): Counter arrangement according to claim 7, further comprising:

- an incrementer/decrementer unit having a control input for selecting an increment or a decrement function;

- a first select switch for coupling the incrementer/decrementer unit with one of the first, second, or third registers;

- an EXCLUSIVE OR gate having two inputs and an output, whereby the first input is coupled with the least significant bit of the first register and the second input is coupled with the least significant bit of the second register;

- a second select switch functionally coupled with the first select switch for coupling the output of the EXCLUSIVE OR gate, the least significant bit of the first register or a logical 0 with the control input of the incrementer/decrementer unit.

12. (original allowed): Counter arrangement according to claim 7, further comprising:

- a seventh, eighth, and ninth register;

- a first and second controllable inverter unit for either inverting or non-inverting a signal; and

- an EXCLUSIVE OR gate having two inputs and an output; whereby

- the first register is coupled with the seventh register;

- the second register is coupled through the first inverter unit with the eighth register;

- the third register is coupled through the second inverter unit with the ninth register; and whereby

- the least significant bit of the first register is coupled with the first input of the EXCLUSIVE OR gate and with the control input of the first inverter unit; and

- the least significant bit of the second register is coupled with the second input of the EXCLUSIVE OR gate whose output is coupled with the control input of the second inverter unit.

13. (original allowed): Counter arrangement according to claim 12, further comprising:

- a third and fourth controllable inverter unit; wherein

- the seventh register is coupled with the first register;

- the eighth register is coupled through the third inverter unit with the second register;

- the ninth register is coupled through the fourth inverter unit with the third register; and whereby

- the least significant bit of the seventh register is coupled with the control input of the third inverter unit; and

- the least significant bit of the eighth register is coupled with the control input of the fourth inverter unit.

14. (original allowed): Counter arrangement according to claim 13, wherein the seventh, eighth and ninth registers are concatenated and further comprising an incrementer/decrementer unit coupled with the concatenated registers.

Claims 15-26 (canceled)